REMARKS

New Claim

Applicant has added new claim 10, which depends from amended claim 1.

Formal Objection and §112 Rejections

The Examiner has raised a formal objection to the phrase "is likely to," as recited in claims 1-9,[1] e.g. in the limitation "determining whether or not the buffer memory is in a state in which buffer underrun is likely to occur..." as recited in claim 1. In particular, the Examiner regards limitations with the phrase "is likely to" as not reciting a positive step. The Applicant has amended the claims to more positively recite steps. The phrase "buffer underrun warning state" has been added in claims 1, 4, 5, and 6. No new matter has been added. (See, e.g., p. 10 line 30 – p. 11 line 7, in which a buffer underrun warning state may be determined based on the data amount in the buffer memory.) The determination of a buffer underrun warning state is a positive step, based on determining the amount of data stored in the buffer memory. By way of example only, a buffer underrun warning state may be determined when at least one sector of data is still in the buffer memory. (See p. 15, lines 20-22.)

The Examiner has rejected claims 1-9 under 35 U.S.C. §112, first paragraph. In particular, the Examiner finds no enabling disclosure of "if the laser beam is continuously generated at the relatively low power level" as recited in claim 1.[2]

The interrupt/restart circuit controls the laser drive circuit so that a drive signal having a constant voltage is output from the laser drive circuit. This results in the optical head irradiating the optical disc with a relatively low power level laser beam. Thus, the circuitry that provides for the relatively low power level is the laser drive circuit.

The Examiner also asserts that there is no disclosed circuitry that provides for the detection of the buffer underrun condition. To the contrary, the buffer underrun

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[1] Applicant notes that the text of the Office Action refers to claims 1-5 and 7-10 being objected to. However, there is no pending claim 10, and the objectionable phrase appears in all the currently pending independent claims, including claim 6.

[2] Applicant notes that this exact phrase is not found in independent claims 4, 5, or 6. The Applicant infers that Examiner is objecting to similar phrases found in those claims. Applicant believes the following remarks will be equally applicable to all the claims. If the Examiner does not agree, it is respectfully requested that the Examiner point out all the phrases of the claims which are found objectionable.

determination circuit determines the amount of data stored in the buffer memory from the address at which writing or reading is presently performed. Based on the data amount, the buffer underrun determination circuit determines whether or not the buffer memory is in a state in which buffer underrun may occur. Thus, the circuitry that provides for the detection of the buffer underrun condition is the buffer underrun determination circuit.

Finally, concerning the Examiner's "interpretation" of Applicant's invention,[3] Applicant maintains that the invention is explicated by the pending claims. Any interpretation of the invention which deviates from or falls short of the claims is necessarily inaccurate or incomplete.

Rejections over Prior Art

Examiner has rejected claims 1-3, 4-6, and 9 over JP-08-147879 (Murata) (alternatively referred to as JP-2842262 in previous office actions) in view of either Takagi et al[4] or EP 507571 (Shimizu). Examiner maintains however that Murata discloses "in this environment the ability to stop recording/interrupt laser power, upon an appropriate buffer condition," and concedes that Murata does not disclose "the ability of having a memory addressing ability so as to know at which location the system was interrupted, and subsequent resumption occurs at the proper location." Examiner maintains that either Takagi or Shimizu discloses the limitations of the rejected claims which are not disclosed by Murata.

First, we submit that the combination of Murata with either Takagi or Shimizu is improper. In the following, citations to Murata refer to the pages in the attached translation. Murata discloses writing data from a host computer 10 to an optical disk. (p. 8, 2nd paragraph). Before being written to the optical disk, the data is stored in a data buffer 14. A

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[3] "As interpreted by the examiner applicant's invention is drawn to interrupt ability for recording when two conditions exist: a) buffer underrun condition, b) presence of sync signal." Office Action p. 3

[4] The Applicant notes that there are at least two prior art references of record corresponding to "Takagi et al." Namely, U.S. Patents 6,115,337 and 5,910,935. They will collectively be referred to as "Takagi" below; the Applicant believes the following comments are equally applicable to either Takagi reference. In the future, it is respectfully requested that the Examiner unambiguously identify the prior art references on which his comments are based. See 37 C.F.R. §1.104(d)(1) ("If domestic patents are cited by the examiner, their numbers and dates, and the names of the patentees will be stated. If domestic patent application publications are cited by the examiner, their publication number, publication date, and the names of the applicants will be stated. If foreign published applications or patents are cited, their nationality or country, numbers and dates, and the names of the patentees will be stated, and such other data will be furnished as may be necessary to enable the applicant, or in the case of a reexamination proceeding, the patent owner, to identify the published applications or patents cited.")

data amount detector 34 detects the amount of data stored in the data buffer during the recording mode. (p. 9 paragraph 3). The data is written to the optical in pre-determined unit sections (e.g. packets or tracks; see p. 12, paragraph 1.) In operation, Murata:

> detects whether substantially the entire data of the next unit section is stored in the buffer memory at a timing right before the start of recording of a unit section (one packet in Incremental Writing, and one track in Track at Once) on which interleaving is performed. If substantially the entire data of the next unit section is detected, the recording is continued, and if not detected, the recording is interrupted and is suspended until the [sic] substantially the entire data is stored to resume recording. This prevents buffer empty from occurring in the middle of recording the unit section.

(Murata, p. 12, paragraph 1). Thus, in the event of an interrupt, Murata *automatically* knows the location where the interrupt took place, since interrupts only occur between unit sections. Therefore, it would be completely unnecessary to modify the Murata system to account for a memory address where the interrupt occurred. Therefore, the combination is improper. Indeed, in combining references under §103(a), "[t]he question is whether there is something in the prior art as a whole to suggest the *desirability*, and thus the obviousness, of making the combination...." In re Fulton, 391 F.3d 1195, 1200 (Fed. Cir. 2004) (emphasis in original); see also MPEP §2143.01(I).

Absent such a desirability, it appears the Examiner is making a "hindsight reconstruction," using applicant's claim as a template to reconstruct the invention by picking and choosing isolated disclosures from the prior art. This is impermissible under the law. For example, in In re Fritch, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1784 (Fed. Cir. 1992), the Federal Circuit stated:

> It is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious. In re Gorman, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed. Cir. 1991). This court has previously stated that "[o]ne cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention." (quoting In re Fine, 837 F.2d at 1075, 5 USPQ2d at 1600)

The present rejection fits the court's description of what may not be done under §103. The Examiner has merely listed certain components of applicant's invention and then located isolated disclosures of those components. The law requires more than that.

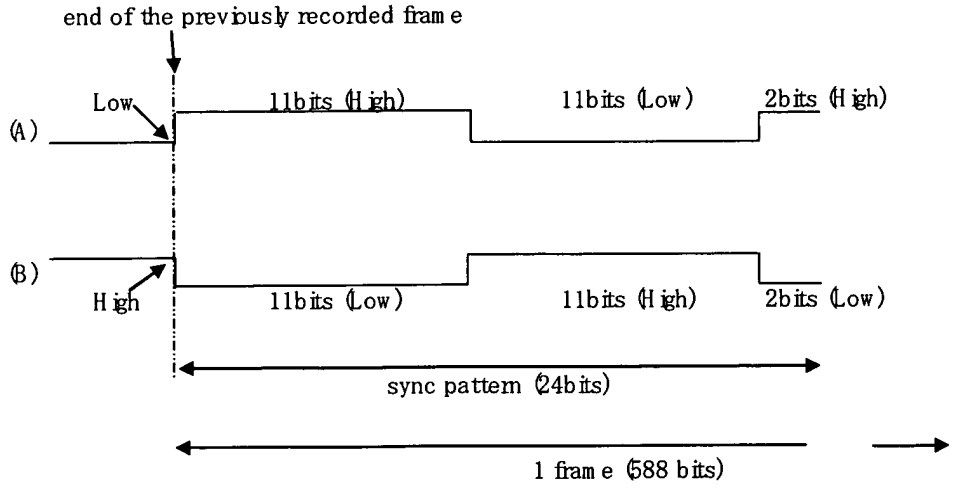
The Examiner must show where the prior art provides a motivation to combine the references he/she has combined in the obviousness rejection. Absent a motivation to

combine, obviousness has not been demonstrated. As the Federal Circuit stated in Northern Telecom, Inc. v. Datapoint Corp., 908 F.2d 931, 934, 15 USPQ2d 1321, 1323 (Fed. Cir. 1990):

> It is insufficient that the prior art disclosed the components of the patented device, either separately or used in other combinations; there must be some teaching, suggestion, or incentive to make the combination made by the inventor.

Second, even if the combination of Murata with either Shimizu or Takagi were proper, neither combination discloses or suggests a "system control circuit for interrupting data recording only if the laser beam is generated at the relatively low power level " (emphasis added) as recited in amended claim 1.

Murata discloses interrupting data recording at a timing in which data recording of the currently recording unit (packet) ends when the buffer memory is in a state in which buffer underrun may occur. However, Murata does not disclose interrupting data recording only at a timing in which the laser beam is continuously generated at a low power level. In a CD-R medium, a 24-bits sync pattern data is added to each head of recording unit (frame). The pattern of the 24-bits sync pattern data varies in accordance with the end level of the previously recorded frame. More specifically, the 24-bits sync pattern data has one of the following illustrated two patterns (A) and (B). When the end level of the previously recorded frame is low, the 24-bits sync pattern data has a pattern (A). When the end level of the previously recorded frame is high, the 24-bits sync pattern data has a pattern (B). Thus, in the operation of Murata, data recording may be interrupted when the laser beam is generated at a high power level.



Similarly, claims 4, 5, and 6 have been amended to require an interrupt only when the laser output is at a low level, and the comments made above are similarly applicable to those claims. Thus, the Applicant respectfully requests the rejections made by the Examiner in sections 5 and 6 of the Office Action be withdrawn for the reasons stated above.

With respect to section 7 of the Office Action, Examiner rejected claims 7 and 8 "as being unpatentable over their respective parent claims 6 and 4 respectively as stated above, and further in view of either the acknowledged prior art or Koishi." Although there are at least two references of record corresponding to the name "Koishi," Applicant understands Examiner's comments to refer to U.S. Patent no. 4,546,462. Furthermore, Applicant understands the Examiner to mean that claims 7 and 8 are rejected over *the prior art* which was cited in the rejection of claims 6 and 4. Applicants therefore submit that the comments made with regard to claims 4 and 6 also demonstrate the patentability of claims 7 and 8.

All of the dependent claims are patentable for at least the reasons for which the claims on which they depend are patentable. Canceled claims, if any, have been canceled without prejudice or disclaimer.

Any circumstance in which the applicant has (a) addressed certain comments of the Examiner does not mean that the applicant concedes other comments of the Examiner, (b) made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims, or (c) amended or canceled a claim does not mean that the applicant concedes any of the Examiner's positions with respect to that claim or other claims.

Enclosed is a $120 check for the Petition for Extension of Time fee. Please apply any other charges or credits to deposit account 06-1050, referencing Attorney Docket Number 10449-028002.

Respectfully submitted,

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